531 Rec'd PCT/PT 27 DEC 2001

FORM PTO-1390 (REV. 9-2001) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER: 8074-6 (S1638 SB/fis)

U.S. APPLICATION NO. (If known, see 37 CFR 1.5): 10/019885

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/DE00/01735	May 29, 2000	June 30, 1999

TITLE OF INVENTION: Circuit for Generating Clock Pulses in a Communication System

APPLICANT(S) FOR DO/EO/US: Markus Balb; Ralf Schedel; and Walter Fiessinger

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. [X] This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. [ ] This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. [ ] This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include items (5), (6), (9) and (21) indicated below.
4. [X] The US has been elected by the expiration of 19 months from the priority date (Article 31).
5. [X] A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. [X] is attached hereto (required only if not communicated by the International Bureau).
   b. [X] has been communicated by the International Bureau.
   c. [ ] is not required, as the application was filed in the United States Receiving Office (RO/US).
6. [X] An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. [X] is attached hereto.
   b. [ ] has been previously submitted under 35 U.S.C. 154(d)(4).
7. [ ] Amendments to the claims of the International Aplication under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. [ ] are attached hereto (required only if not communicated by the International Bureau).
   b. [ ] have been communicated by the International Bureau.
   c. [ ] have not been made; however, the time limit for making such amendments has NOT expired.
   d. [ ] have not been made and will not be made.
8. [X] An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371 (c)(3)).
9. [ ] An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. [X] An English lanugage translation of the annexes of the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11 to 20 below concern document(s) or information included:

11. [ ] An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. [ ] An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. [X] A FIRST preliminary amendment.
14. [ ] A SECOND or SUBSEQUENT preliminary amendment.
15. [ ] A substitute specification.
16. [ ] A change of power of attorney and/or address letter.
17. [ ] A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821 - 1.825.
18. [ ] A second copy of the published international application under 35 U.S.C. 154(d)(4).
19. [ ] A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
20. [ ] Other items or information:

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U.S. APPLICATION NO. (if known, see 37 CFR 1.5)	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
10/019885	PCT/DE00/01735	8074-6 (S1638 SB/fis)

21. ☒ The following fees are submitted:	CALCULATIONS PTO USE ONLY	
BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)):		
Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO **$1040.00**		
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO **$890.00**		
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO **$740.00**		
International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4) **$710.00**		
International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4) **$100.00**		
ENTER APPROPRIATE BASIC FEE AMOUNT =	$ 890.00	
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	$ 130.00	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total claims	7 - 20 =	0	x **$18.00**	$ 0	
Independent claims	1 - 3 =	0	x **$84.00**	$ 0	
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ **$280.00**	$ 0	
TOTAL OF ABOVE CALCULATIONS =				$ 1,020.00	
☐ Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by 1/2.			+	$ 0	
SUBTOTAL =				$ 1,020.00	
Processing fee of **$130.00** for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(f)).				$ 0	
TOTAL NATIONAL FEE =				$ 1,020.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00** per property +				$ 0	
TOTAL FEES ENCLOSED =				$ 1,020.00	
				Amount to be refunded:	$
				charged:	$

a. ☒ A check in the amount of $ 1,020.00 to cover the above fees is enclosed.

b. ☐ Please charge my Deposit Account No. _____ in the amount of $ _____ to cover the above fees. A duplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 50-0679 . A duplicate copy of this sheet is enclosed.

d. ☐ Fees are to be charged to a credit card. **WARNING:** Information on this form may become public. **Credit card information should not be included on this form.** Provide credit card information and authorization on PTO-2038.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137 (a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

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34,136
REGISTRATION NUMBER

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Attorney Docket: 8074-6 (S1638 SB/fis)

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT(S): Markus Balb et al.

INT'L. APPLN. NO: PCT/DE00/01735

INT'L. FILING DATE: May 29, 2000

FOR: CIRCUIT FOR GENERATING CLOCK PULSES IN A COMMUNICATION SYSTEM

Assistant Commissioner for Patents
Washington, D.C. 20231

EL797416073US

PRELIMINARY AMENDMENT

Sir:

Before examination of the above-identified application on the merits, kindly amend the application as follows:

IN THE CLAIMS:

Please cancel claims 1-10, without prejudice.

Please add the following new claims 11-17:

CERTIFICATION UNDER 37 C.F.R. § 1.10

I hereby certify that this New Application Transmittal and the documents referred to as enclosed therein are being deposited with the United States Postal Service on this date December 27, 2001 in an envelope as "Express Mail Post Office to Addressee" Mail Label Number EL797416073US addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231.

Frank Chau

11. (New) A circuit arrangement for a communication system for terminating a plurality of interfaces at a common bus and for generating a synchronization clock for synchronizing the bus, comprising:

a first multiplexer which can be controlled by a first control signal with a plurality of inputs corresponding to a plurality of transmission lines of the interfaces;

a respective phase control unit, preceding each input of the first multiplexer, which derives a respective clock generator signal from the received signal of the corresponding transmission line;

where the clock generator signal of one of the transmission lines can be switched through as output signal of the first multiplexer in dependence on the first control signal;

a phase locked loop, at the inputs of which the output signal of the first multiplexer and a clock from a clock generator which can be operated with an external oscillating crystal, are present and at the output of which an internal reference clock is present which is generated from the clock generator signal and the clock from the clock generator;

an output connection for the clock from the clock generator;

a second multiplexer, which can be controlled by a second control signal, at the inputs of which the output signal of the phase locked loop and a reference clock, which can be supplied externally, are present;

where one of the input signals of the second multiplexer can be switched through as output signal of the second multiplexer in dependence on the second control signal;

a clock divider unit, following the second multiplexer for generating the synchronizing clock from the output signal of the second multiplexer.

12. (New) The circuit arrangement as claimed in claim 11, characterized in that the clock generator signal can be generated by a combination of the received signals of at least two transmission lines of the interfaces, particularly by averaging.

13. (New) The circuit arrangement as claimed in claim 11, characterized in that signals which can be transmitted via the transmission lines of the interfaces correspond to the U interface protocol of ISDN.

14. (New) The circuit arrangement as claimed in claim 12, characterized in that signals which can be transmitted via the transmission lines of the interfaces correspond to the U interface protocol of ISDN.

15. (New) The circuit arrangement as claimed in claim 11, characterized in that signals which can be transmitted via the transmission lines of the interfaces correspond to an XDSL protocol.

16. (New) The circuit arrangement as claimed in claim 12, characterized in that signals which can be transmitted via the transmission lines of the interfaces correspond to an XDSL protocol.

17. (New) The circuit arrangement as claimed in claim 15, characterized in that the XDSL protocol corresponds to an ADSL or SDSL or VDSL or HDSL protocol.

REMARKS

Before examination on the merits of the above application, please enter the present Preliminary Amendment. Early and favorable reconsideration is respectfully requested.

Respectfully submitted,

By: _____
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Circuit arrangement for generating clock pulses in a communication system

The invention relates to a circuit arrangement for generating clock pulses in a communication system as claimed in the preamble of claim 1.

In ISDN (Integrated Services Digital Network), the connection at the subscriber end, the so-called ISDN basic access, have a number of reference points R, S, T, U which correspond to interfaces.

Figure 1 shows a model of the ISDN basic access with a connection to an exchange. The U interface forms the line termination both at the subscriber end and at the exchange end.

The exchange have a local line termination 2 (LT) and a digital ISDN exchange termination 1 (ET) which communicate with one another via the V interface.

The ISDN basic access have a network termination 3 (NT) at the subscriber end. The network termination 3 is composed of a first network termination 7 (NT-1), which transfers user information and signaling information to the exchange (physical network termination according to level 1 of the ISO/OSI reference model), and a second network termination 8 (NT-2) which handles concentrating and switching tasks (logical network termination according to level 2 and 3 of the ISO/OSI reference model). The first and second network terminations 7, 8 are connected via the T interface.

A digital ISDN-compatible subscriber terminal 4 (TE1) can be connected directly to the second network termination 8 via the S interface.

To connect an analog subscriber terminal 6 (TE2), a terminal adapter 5 (TA) is necessary which is connected to the second network termination 8. The analog subscriber terminal 6 can then be connected to the terminal adapter 5 via the R interface.

In the ISDN basic access, hierarchical clock synchronization is used: a device configured as master, for example a device executing the top levels of the ISO/OSI reference model, synchronizes a device configured as slave, for example a device executing the lower levels of the ISO/OSI reference model.

In figure 1, the exchange 2 is configured as master of the network termination 3 and synchronizes it.

In the case of a multiplicity of slaves which are synchronized by a master, one of these slaves is appointed as reference clock generator for the remaining slaves. In the case of a failure of the reference clock generator, a further slave is appointed as reference clock generator and so forth.

Figure 2a shows an arrangement in which, at the subscriber end in an ISDN basic access, a number of first network terminations 12 to 14 are connected to a telecommunication system 15 via a common network termination system bus 18. The telecommunication system 15 have the further elements of the ISDN basic access of the subscriber end. A number of subscriber terminals 16 to 17 can be connected to the telecommunication system 15. The first network terminations 12 to 14 are in each case connected to local exchange terminations 9 to 11 via a U interface.

For the hierarchical clock synchronization, the first network terminations 12 to 14 execute tasks of the same

level of the ISO/OSI reference model so that one of the first network terminations 12 to 14 or, respectively, one of the corresponding U interfaces must be selected as first reference clock generator for the remaining first network terminations or, respectively, U interfaces. Furthermore, further reference clock generators must be determined which take over the task of the first reference clock generator in the event of its failure. The network termination system bus 18 must be synchronized to the respective reference clock generator.

Figure 2b shows in detail the clock generation and distribution of various clocks in the arrangement pictured in figure 2a. The clocks necessary for operating the arrangement are generated via a phase locked loop 100 and a clock divider 101. To illustrate the direction of synchronization, a line termination 16 (LT) of the network operator, which is responsible for the synchronization, is shown diagrammatically on the right-hand side in figure 2b. Furthermore, a network termination with subscriber terminal NT/TE 17 is shown by way of example on the left-hand side.

Each of the first network terminations 12 to 14 have its own 15.36 MHz crystal by means of which, for example, a 512 kHz clock CLS is generated as reference clock. The clock CLS is supplied to the phase locked loop 100 which, in turn, generates from the 512 kHz clock a 15.36 MHz clock XIN, an 8 kHz frame clock FSC and a bit clock DCL which has a frequency of between 512 and 4096 kHz. The frame clock FSC and the bit clock DCL are supplied to each of the first network terminations 12 to 14 and each of the local exchange terminations 9 to 11 via in each case one line. The clock XIN is fed back to the phase locked loop 100 via the clock divider 101 and supplied in parallel to the

local exchange terminations 9 to 11 via one line. In this arrangement, the reference clock generator is the 512 kHz clock CLS which is generated in each of the first network terminations 12 to 14.

Figure 3 shows an arrangement in which a line termination 20 which is not ISDN capable provides subscribers with access to the public ISDN network by means of a digital loop carrier (DLC) system.

For this purpose, a number of first subscriber accesses 35 are combined in a first so-called "D-channel bank" 22 in a digital ISDN exchange termination 19. The basic channels of each basic access are transmitted concentrated to the line termination 20 via a first broadband transmission channel 23.

In the line termination 20, the basic channels of a second "D-channel bank" 24 are distributed to the corresponding subscriber accesses 25 to 32 which are also called line cards in technical language. A number of accesses 25 to 28 are then combined in a third "D-channel bank" 21 to form so-called "central office terminals" and are transmitted via a second broadband transmission channel 33 to a subscriber having a number of network terminations 36 to 37.

The individual accesses 25 to 28 are there distributed to the corresponding network terminations via a fourth "D-channel bank" 34 which forms the so-called remote digital terminal (RDT).

The arrangements shown in figures 2 to 3 can also be used for so-called xDSL (x Digital Subscriber Line) systems such as ADSL, SDSL, VDSL or HDSL. It is only necessary to replace the ISDN transmission method at the U interfaces by the corresponding xDSL transmission

method. The basic arrangement shown in figures 2 to 3 will not change.

In the arrangement shown in figure 3, similarly to the arrangement shown in figure 2, a reference clock generator must be selected and other reference clock generators used as replacement in the event of a failure of the first reference clock generator must be determined for the hierarchical clock synchronization.

The invention is, therefore, based on the object of creating a circuit arrangement for generating clock pulses in a communication system which, in particular, is based on ISDN or xDSL, in which the disadvantages described initially are avoided and, in particular, the circuit arrangement can be connected directly to a telecommunication system or a concentrator via a common network termination system bus.

This object is achieved by a circuit arrangement having the features of claim 1. Preferred embodiments of the invention are the subject matter of the dependent claims.

The circuit arrangement for generating clock pulses in a communication system according to the invention have at least one network termination, where each network termination can be connected to at least one transmission line in each case and to a bus and where a clock is provided for synchronizing the bus. A multiplicity of clock generators for generating the clock and means for selecting a clock generator are provided in the circuit arrangement. The circuit arrangement can be advantageously connected to a telecommunication system via the bus without any additional circuit expenditure.

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The means for selecting a clock generator are preferably programmable. Furthermore, the means for selecting a clock generator can be programmable via a register. Due to the programming, the circuit arrangement can be adapted to various requirements and, in particular, in the event of a failure of one of the clock generators, is still operational by means of simple reprogramming.

The means for selecting a clock generator preferably has a first multiplexer, to whose inputs transmission lines can be connected, particularly via so-called phase control units, and a signal from which a clock is derived is received via one of the transmission lines. In other words, the received signals of the connected transmission lines are used as clock generator, as it were, and the phase control units extract the clock information from the signal received in each case. In particular, the means for selecting a clock generator has a second multiplexer, at the inputs of which the output signal of a phase locked loop and a reference clock are present. The phase locked loop is preferably supplied with a further clock from a crystal oscillator circuit and the output signal of the first multiplexer as input signals.

In a preferred embodiment, the following three clock generators can be used as reference clock generators: a signal received via one of the transmission lines is used as first clock generator, the reference clock itself is used as second clock generator if all transmission lines are in active, and the combination of received signals from at least two transmission lines is used as third clock generator, the clock generated by the third clock generator being generated, in particular, by averaging the clock information determined from the signals of the transmission lines

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involved. The averaging for determining the clock can also be provided with weighting. The signals of all four transmission lines are preferably combined in order to derive the clock information for the reference clock.

The signals which are transmitted via the transmission lines preferably correspond to the U interface protocol of ISDN. The circuit arrangement can then be advantageously used in ISDN applications in which a number of U interfaces are administered.

On the other hand, the signals which are transmitted via the transmission lines can also correspond to an XDSL protocol. For this purpose it is only necessary to change the signal transmission method to an XDSL transmission method. In particular, the XDSL protocol can correspond to an ADSL or SDSL or VDSL or HDSL protocol.

Preferred embodiments of the invention are found in the subsequent description in conjunction with the drawings, in which:

Figure 1 shows a model of the ISDN basic access with a connection to an exchange,

Figure 2a shows an arrangement in which at the subscriber end in an ISDN basic access, a number of first network terminations are connected to a telecommunication system via a common network termination system bus,

Figure 2b shows the clock generation and distribution in the arrangement shown in figure 2a,

Figure 3 shows an arrangement in which a line

termination provides subscribers with access to the public ISDN network by means of a digital loop carrier (DLC) system,

Figure 4 shows a first exemplary embodiment of a circuit arrangement according to the invention, and

Figure 5 shows a second exemplary embodiment of a circuit arrangement according to the invention.

Figures 1 to 3 which relate to the prior art have already been discussed in the introduction to this description.

Figure 4 shows an integrated circuit 40 which have four U interfaces 41 to 44. The integrated circuit 40 is used in a communication system for connecting four U interfaces to a common network termination system bus which, in turn, can be connected to a telecommunication system.

An external reference clock 46 which is generated, for example, by another integrated circuit, can be fed into the integrated circuit 40. This external reference clock 46 is needed when none of the four U interfaces are active and accordingly no U interface is available as reference clock generator.

Each of the four U interfaces 41 to 44 can be programmed as reference clock generator. For this purpose, the integrated circuit 40 have a first multiplexer 47 which can be controlled via a first control signal 45. To extract a clock signal from the respective received signals of the U interfaces 41, 42, 43, 44, the multiplexer 47 in each case have a phase control unit (PCU) 66, 67, 68, 69 for each input. The first control signal 45 switches one of the four U

interfaces 41 to 44, which are connected to the inputs of the first multiplexer 47, through to the output of the first multiplexer 47. The output signal of the multiplexer 47 is conducted to a phase locked loop 48 which receives a clock of 15.36 MHz via a clock generator 55. The 15.36 MHz clock is available as output signal 54, for example for other integrated circuits. The clock generator 55 can be connected to a 15.36 MHz crystal 58 via connections 56 and 57. From the signals received via a U interface operating as reference clock generator, the phase locked loop 48 regenerates the reference clock which is supplied to a second multiplexer 49. The second multiplexer 49 is switched by a second control signal 51. The second multiplexer switches either the reference clock regenerated from a U interface or the external reference clock 46 fed in if none of the four U interfaces are active, through to a PLL/clock divider unit 50. The PLL/clock divider unit 50 divides a first clock at its input into a second clock 52 and a third clock 53. The second clock 52 can be used for synchronizing a network termination system bus and have an 8 kHz frame clock FSC. The third clock 53 have a bit clock DCL. Furthermore, the PLL/clock divider unit 50 uses the clock generated by the clock generator 55.

The integrated circuit 40 can be programmed as master or as slave. This makes it possible to set the direction of synchronization of an arrangement in which the integrated circuit 40 is used. In master mode, the reference clock generator can be set to one of the following clock sources by programming the integrated circuit 40:

- one of the four U interfaces 41 to 44 is used as reference clock generator; or
- the mean value over all four U interfaces 41 to 44 is formed; the mean value is then used as reference

clock generator; or

- an external reference clock 46 is used as reference clock generator; this setting is appropriate if none of the four U interfaces 41 to 44 are active.

Figure 5 shows these three cases of operation.

A first 59, second 60 and third 61 integrated circuit as shown in figure 4 are interconnected to form a chain and are used for driving a total of twelve U interfaces U1 to U12.

The first integrated circuit 59 is configured as master. For this purpose, a 15.36 MHz crystal 62 is connected to the first integrated circuit 59. By this means, a 15.36 MHz clock is generated internally which is conducted as clock signal 62 to a connection XIN of the second integrated circuit 60 provided for connecting a crystal. As a result, the second integrated circuit does not need a crystal. The U interfaces U1 to U4 connected to the first integrated circuit 59 are all inactive, i.e. no signal is transmitted or received via these interfaces. None of the U interfaces U1 to U4 can thus be used as reference clock generator.

Of the U interfaces U5 to U8 connected to the second integrated circuit 60, U6 and U8 are active, i.e. a signal is transmitted or received via these two interfaces. The second integrated circuit 60 is programmed in such a manner that U interface U8 is to be used as reference clock generator. For this purpose, the reference clock signal 64, which is generated internally in the second integrated circuit 60 via the U interface U8, is conducted as external reference clock to the first integrated circuit 59, the master. The first integrated circuit 59 is programmed for an

external reference clock for this purpose.

The third integrated circuit 61 is supplied with the 15.36 MHz clock 63 at the terminal XIN provided for connecting a crystal from the second integrated circuit 60. In this integrated circuit, too, a crystal is saved. If at least one of the U interfaces U9 to U12 connected to the third integrated circuit 61 is active, i.e. a signal is received or transmitted via one of the U interfaces, the third integrated circuit is programmed as standby reference clock generator for the second integrated circuit 60. For this purpose, the reference clock 65 is conducted to the second integrated circuit 60 as external reference clock from the third integrated circuit 61. The second integrated circuit 60 and third integrated circuit 61 are configured as slaves and accordingly receive the frame clock FSC and the bit clock DCL from the first integrated circuit 59.

The second integrated circuit is programmed as reference clock generator but can be reprogrammed to the external reference clock from the third integrated circuit 61 if all connected U interfaces U5 to U8 fail. For this purpose, a circuit for monitoring the U interfaces can be provided which automatically sets the reference clock generator, i.e. reprograms the second integrated circuit in this case.

Patent Claims

1. A circuit arrangement for generating clock pulses in a communication system, the circuit arrangement (40) hasing at least one network termination (12 to 14), where each network termination (12 to 14) can be connected to at least one transmission line in each case and to a bus (18) and where a clock is provided for synchronizing the bus (18), characterized in that a multiplicity of clock generators (58, 41 to 44, 46) for generating the clock and means (47, 49) for selecting a clock generator (58, 41 to 44, 46) are provided.

2. The circuit arrangement as claimed in claim 1, characterized in that the means (47, 49) for selecting a clock generator (58, 41 to 44, 46) are programmable.

3. The circuit arrangement as claimed in claim 2, characterized in that the means (47, 49) for selecting a clock generator (58, 41 to 44, 46) are programmable via a register.

4. The circuit arrangement as claimed in one of claims 1 to 3, characterized in that the means (47, 49) for selecting a clock generator (58, 41 to 44, 45) has a first multiplexer (47), to whose inputs transmission lines can be connected and where the received signal of one of the transmission lines is used as clock generator.

5. The circuit arrangement as claimed in claim 4, characterized in that the circuit arrangement in each case have a phase control unit (PCU) preceding each input of the multiplexer, which derives a clock from the received signal of the

corresponding transmission line.

6. The circuit arrangement as claimed in claim 4 or 5, characterized in that the means (47, 49) for selecting a clock generator (58, 41 to 44, 46) has a second multiplexer (49), at the inputs of which the output signal of a phase locked loop (48) and a reference clock Refclk (46) are present.

7. The circuit arrangement as claimed in claim 6, characterized in that the phase locked loop (48) is supplied with a further clock from a crystal oscillator circuit (55 to 58) and the output signal of the first multiplexer (47) as input signals.

8. The circuit arrangement as claimed in one of claims 6 or 7, characterized in that three clock generators are provided, where a signal received via one of the transmission lines (41, 42, 43, 44) is used as first clock generator, the reference clock (46) is used as second clock generator and the combination of received signals from at least two transmission lines (41, 42, 43, 44) is used as third clock generator, where the clock generated by the third clock generator is generated, in particular, by averaging the clock information determined from the signals of the transmission lines (41, 42, 43, 44) involved.

9. The circuit arrangement as claimed in one of the preceding claims, characterized in that signals which are transmitted via the transmission lines (41, 42, 43, 44) correspond to the U interface protocol of ISDN.

10. The circuit arrangement as claimed in one of

claims 1 to 8, characterized in that signals which are transmitted via the transmission lines (41, 42, 43, 44) correspond to an XDSL protocol.

11. The circuit arrangement as claimed in claim 10, characterized in that the XDSL protocol corresponds to an ADSL or SDSL or VDSL or HDSL protocol.

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(12) NACH DEM VERTRAG ÜBER DIE INTERNATIONALE ZUSAMMENARBEIT AUF DEM GEBIET DES PATENTWESENS (PCT) VERÖFFENTLICHTE INTERNATIONALE ANMELDUNG

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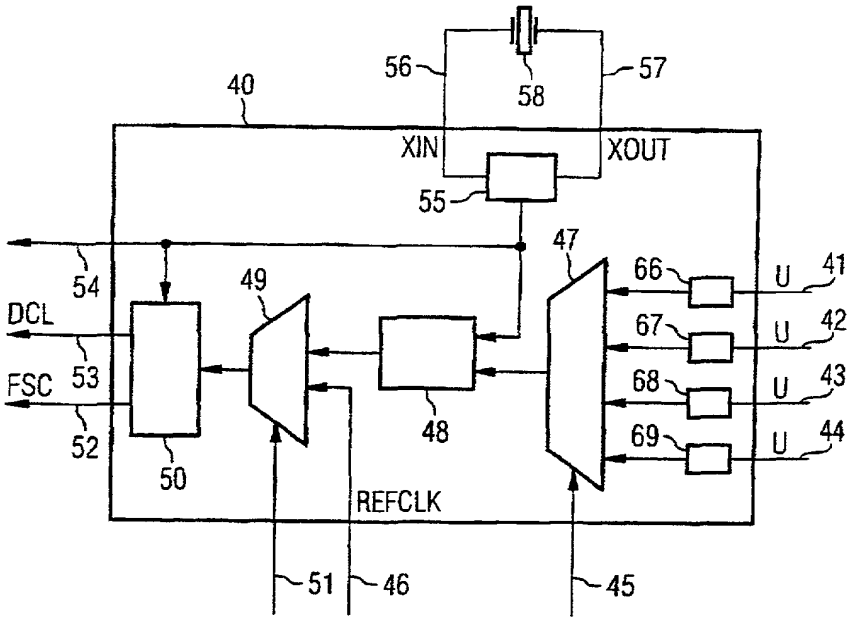
Veröffentlicht:
— *Mit internationalem Recherchenbericht.*

[Fortsetzung auf der nachsten Seite]

(54) **Title:** CIRCUIT FOR GENERATING CLOCK PULSES IN A COMMUNICATIONS SYSTEM

(54) **Bezeichnung:** SCHALTUNGSANORDNUNG ZUR TAKTERZEUGUNG IN EINEM KOMMUNIKATIONSSYSTEM



(57) **Abstract:** The invention relates to a circuit for generating clock pulses in a communications system. Said circuit has at least one network termination. Each network termination can be connected to at least one transmission line and to a bus, respectively and a clock pulse is provided for synchronizing the bus. According to the invention, a plurality of clock pulse generators are provided in the circuit for generating the clock pulse and means is provided for selecting a clock pulse generator.

[Fortsetzung auf der nächsten Seite]

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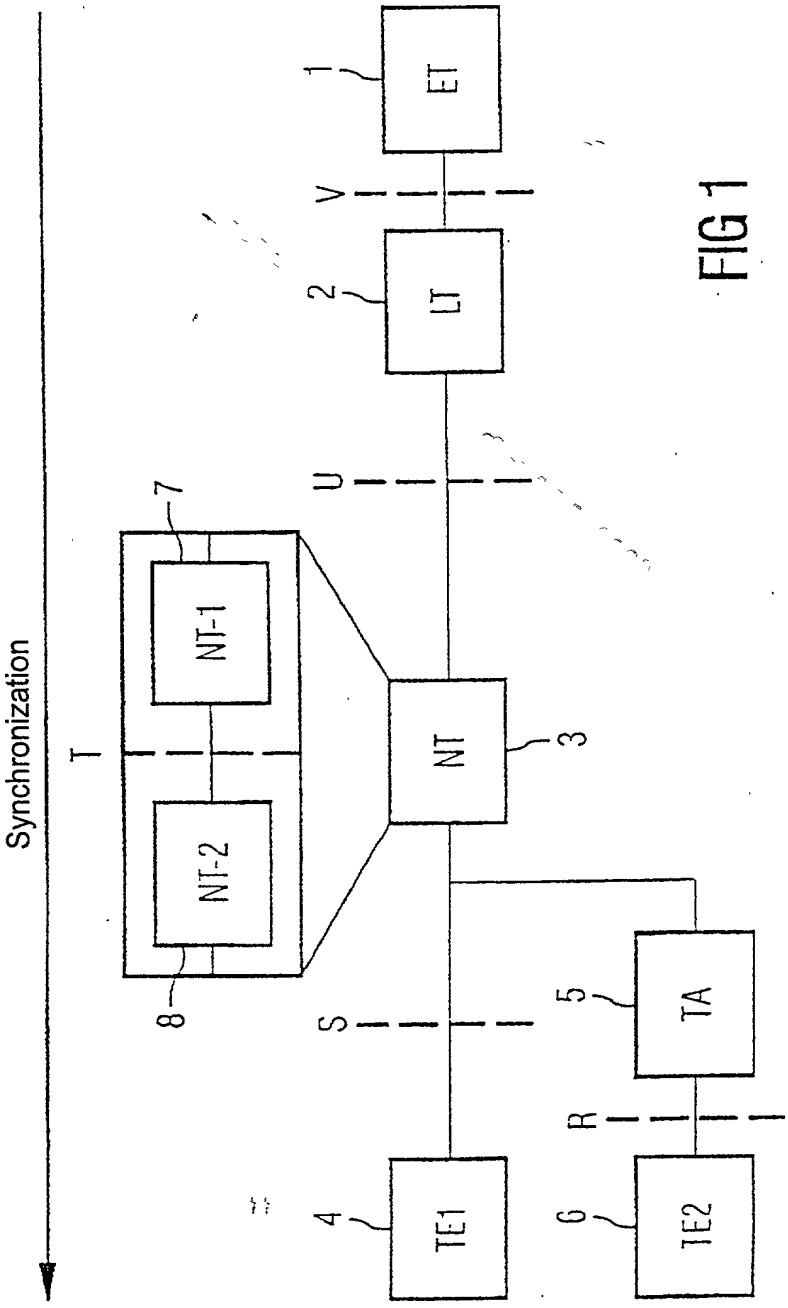

FIG 1

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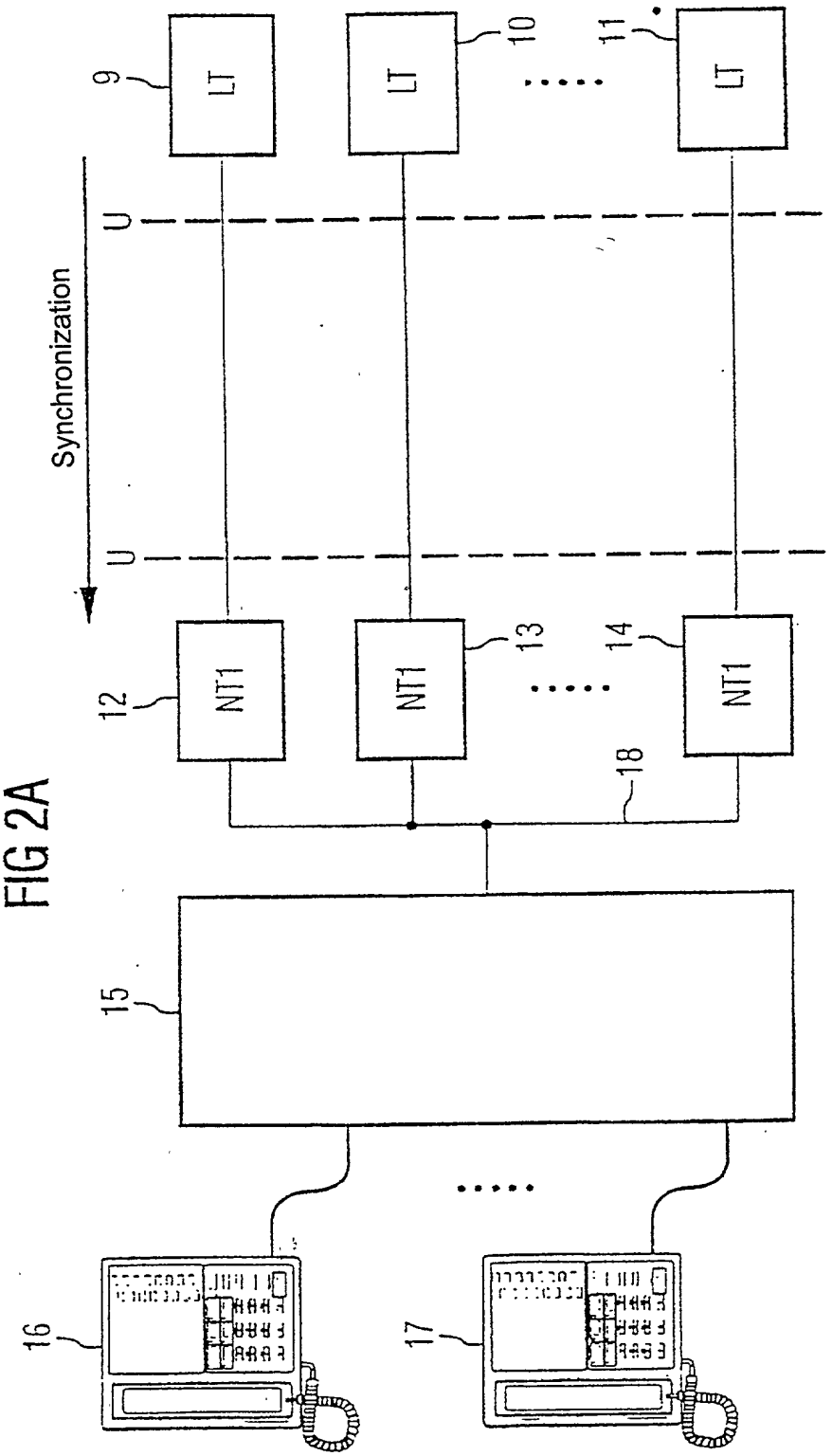

FIG 2A

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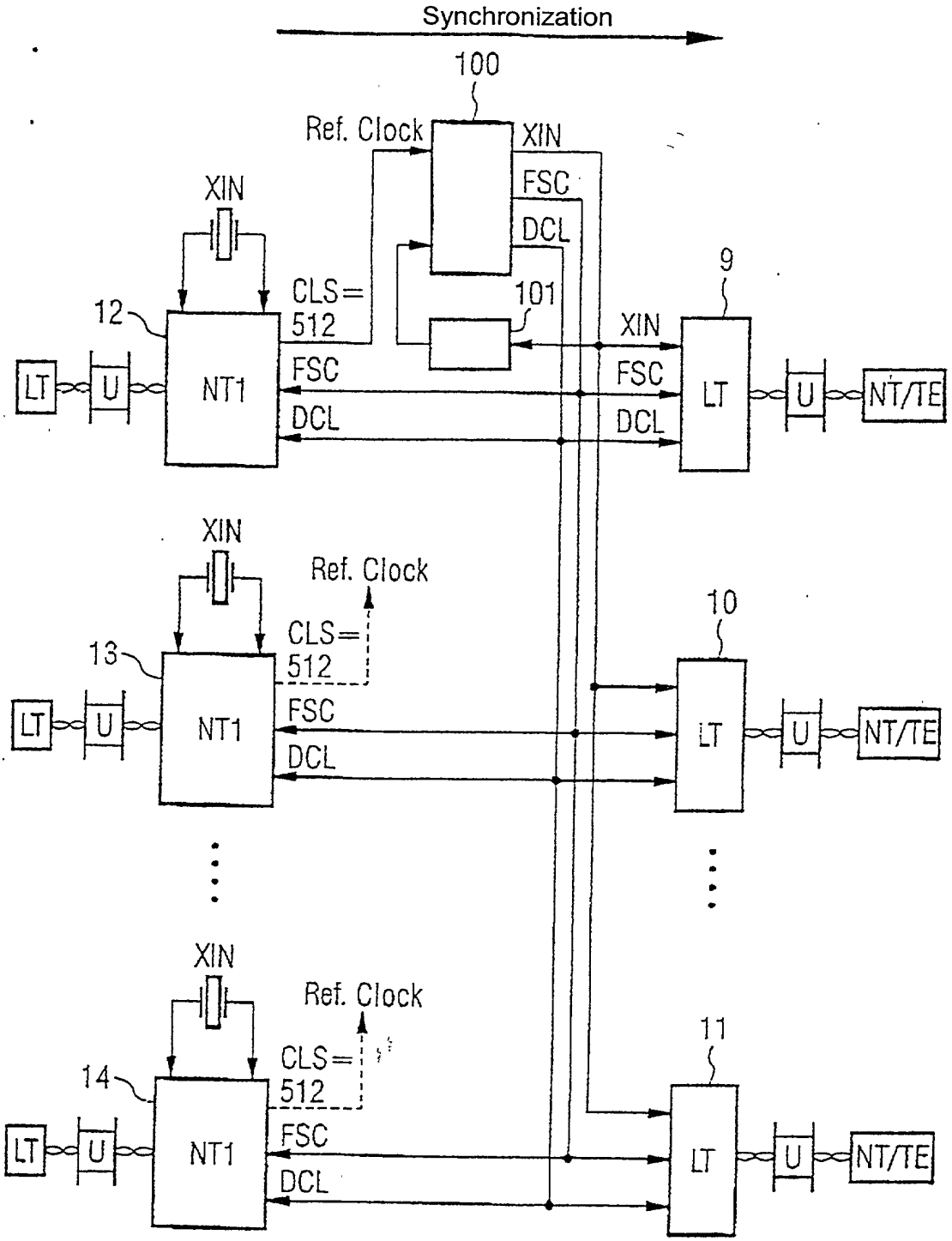
FIG 2B


Synchronization
100
Ref. Clock
XIN
FSC
DCL
101
XIN
CLS=
512
12
NT1
LT
U
FSC
DCL
9
XIN
FSC
DCL
LT
U
NT/TE
XIN
Ref. Clock
CLS=
512
13
NT1
LT
U
FSC
DCL
10
LT
U
NT/TE
XIN
Ref. Clock
CLS=
512
14
NT1
LT
U
FSC
DCL
11
LT
U
NT/TE

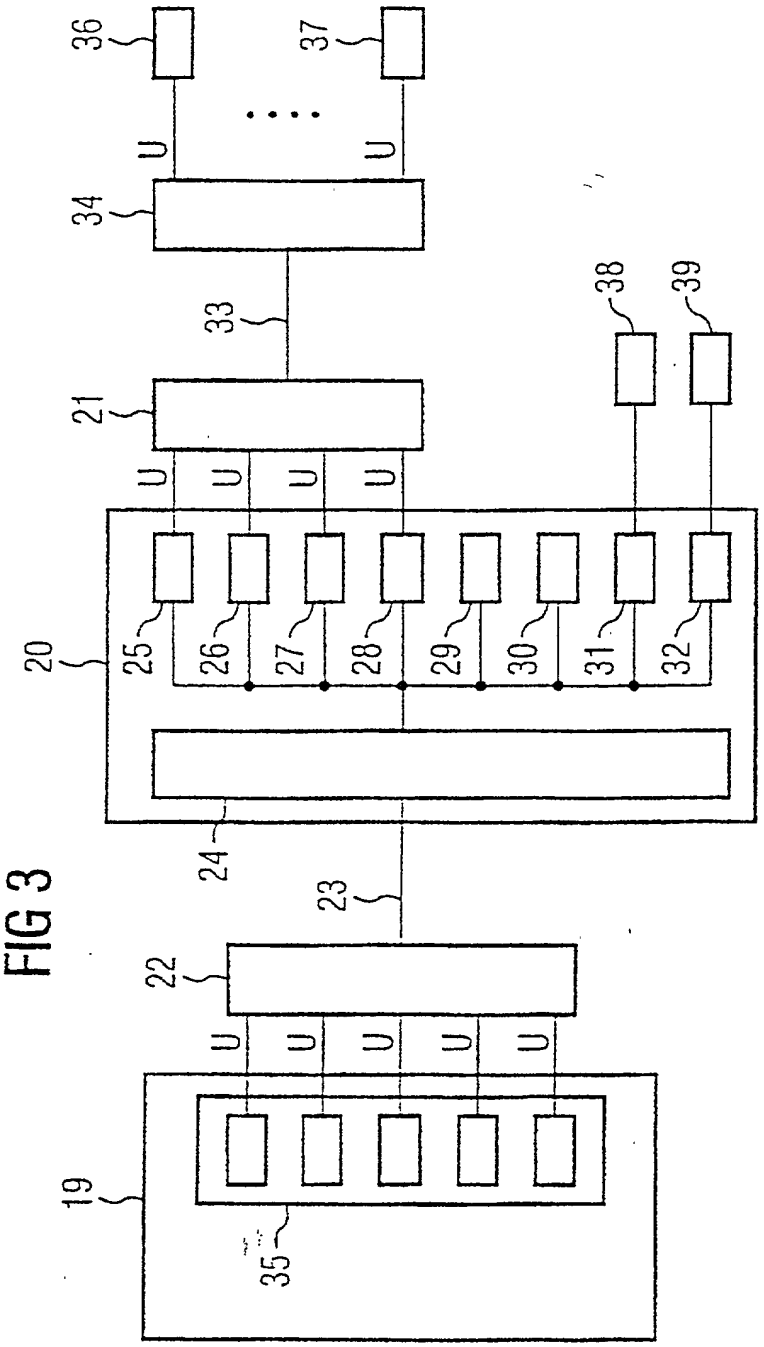


FIG 3

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FIG 4

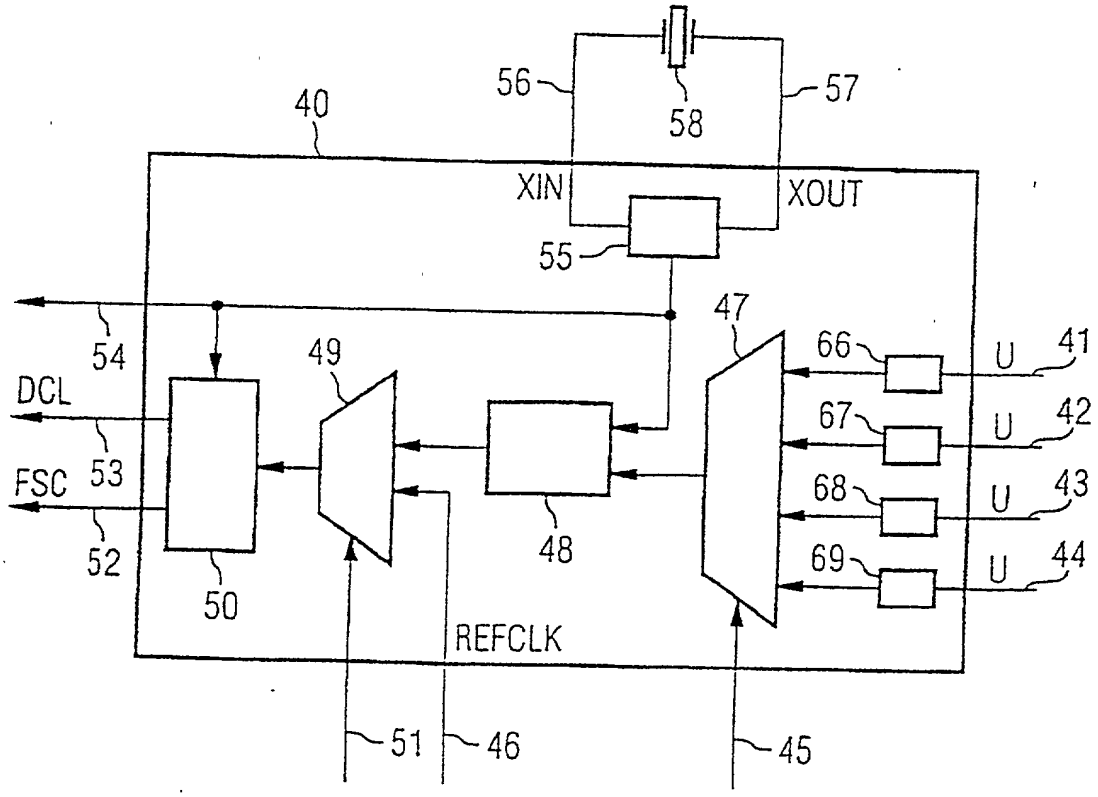
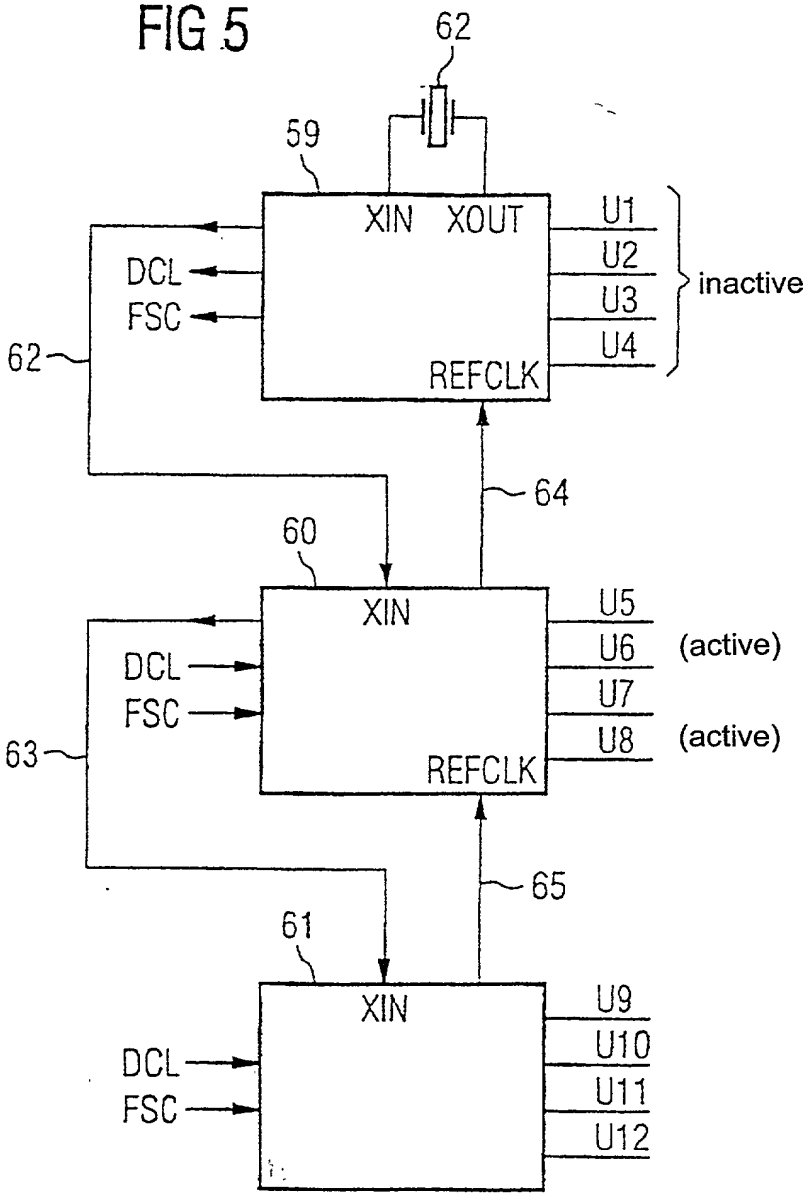

40
56
58
57
XIN
XOUT
55
54
47
49
66
U
41
DCL
67
U
42
53
FSC
68
U
43
52
48
69
U
44
50
REFCLK
51
46
45

FIG 5


62
59
XIN
XOUT
U1
U2
U3
U4
inactive
DCL
FSC
62
REFCLK
64
60
XIN
U5
U6
(active)
U7
U8
(active)
DCL
FSC
63
REFCLK
65
61
XIN
U9
U10
U11
U12
DCL
FSC

PTO/SB/01 (6/95) **DECLARATION** Docket No. 8074-6 (S1638 SB/fis)

AS A BELOW NAMED INVENTOR, I hereby declare that:

My residence, post office address and citizenship are as stated next to my name.

I believe that I am the original, first and sole *(if only one name is listed below)*, or an original, first and joint inventor *(if plural names are listed below)*, of the subject matter which is claimed and for which a patent is sought on the invention entitled:

TITLE: **CIRCUIT FOR GENERATING CLOCK PULSES IN A COMMUNICATION SYSTEM**

the specification of which either is attached hereto or indicates an attorney docket no. _____, or:

☒ was filed in the U.S. Patent & Trademark Office on December 27, 2001 and assigned Serial No. 10/019,885 ,

☐ and *(if applicable)* was amended on _____.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to patentability and to the examination of this application in accordance with Title 37 of the Code of Federal Regulations §1.56. I hereby claim foreign priority benefits under Title 35, U.S. Code §119(a)-(d) or §365(b) of any foreign application(s) for patent or inventor's certificate, or §365(a) of any PCT International application which designated at least one country other than the United States, or §119(e) of any United States provisional application(s), listed below and have also identified below any foreign applications for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

			Priority Claimed:
199 30 191.3	Germany	30 June 1999	Yes [X] No [ ]
(Application Number)	*(Country)*	*(Day/Month/Year filed)*	
			Yes [ ] No [ ]
(Application Number)	*(Country)*	*(Day/Month/Year filed)*	

I hereby claim the benefit under Title 35, U.S. Code, §120, of any United States application(s), or §365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application(s) in the manner provided by the first paragraph of Title 35, U.S. Code, §112, I acknowledge the duty to disclose information material to patentability as defined in Title 37, The Code of Federal Regulations, §1.56(a) which became available between the filing date of the prior application and the national or PCT International filing date of this application:

(Application Serial Number)	*(Filing Date)*	*(STATUS: patented, pending, abandoned)*
(Application Serial Number)	*(Filing Date)*	*(STATUS: patented, pending, abandoned)*

(6) I hereby appoint the following attorneys: **FRANK CHAU**, Reg. No. 34,136; **FRANK V. DeROSA**, Reg. No. 43,584; **JUAN C. VILLAR**, Reg. No. 34,271; **NATHANIEL T. WALLACE**, Reg. No. 48,909; **ERIC M. PARHAM**, Reg. No. 45,747; and **GEORGE D. MORGAN**, Reg. No. 46,505, each of them of **F. CHAU & ASSOCIATES, LLP**, 1900 Hempstead Turnpike, Suite 501, East Meadow, New York, 11554. to prosecute this application and to transact all business in the U.S. Patent and Trademark Office connected therewith and with any divisional, continuation, continuation-in-part, reissue or re-examination application, with full power of appointment and with full power to substitute an associate attorney or agent, and to receive all patents which may issue thereon, and request that all correspondence be addressed to:

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I HEREBY DECLARE that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under §1001 of Title 18 U.S. Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

1-00
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PTO-1656 Rev. 03-2005

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